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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/490,172
Filing Date: January 22, 2000
Appellant(s): MARR, DEBORAH T.

Shawn W. O'Dowd
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed Jan. 16, 2007 appealing from the Office action mailed Jan. 6, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences, which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,105,127	Kimura	Aug. 15, 2000
5,944,809	Olarig	Aug. 31, 1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-11 and 13-21, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura et al. (U.S. Patent. No. 6,105,127), in view of Olarig et al. (U.S. Patent No. 5,944,809).

Kimura et al's patent (EP 0827071 now U.S. Patent No. 6,105,127) was provided twice by applicant via IDS filed on 10/03/2001 and 08/07/2002.

As to claim 20, Kimura et al. (Thereinafter referred as Kimura) disclosed an apparatus for establish thread priority in a processor [Title; Abstract; Fig. 2] comprising:

a) a memory including Task priority Register (TPR) to store a value to indicate which one of the threads has a higher priority [e.g., Fig (s). 6-7; Fig. 15; col. 8, lines 59 – col. 9, line 8, etc.];

b) a resource allocated between the plurality of threads depending on a priority assigned to each thread in the memory [e.g., Abstract, lines 10-15; the shared resource functional unit, col. 6, lines 19-30; col. 8, lines 17-27].

Kimura does not expressly disclose a counter loaded with a predetermined value by control logic for each thread in the memory, such that the value being selected depending on the priority assigned, and the counter being used to allocate said resource between a plurality of threads.

However, Olarig et al. (hereinafter referred as Olarig) discloses a system providing a counter with a predetermined value [e.g., the 2-bit value counter at col. 6, lines 42-57] for the plurality of threads, said value being selected by control logic [e.g., the interrupted controller schema at col. 4, lines 7-14] depending on the priority assigned to each thread, said counter being used in said allocating operation [e.g., the LOPIC and COPIC processing via round robin arbitration protocol in Abstract; Fig(s) 3,

5 and associated texts; Note: the round robin arbitration protocol is default implemented by a plurality of thread].

Kimura and Olarig are in the same field of endeavor to optimize the performance of the extended multiprocessor system via controlling the interrupt signal flow among a plurality of thread processing. Thus, It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system of Kimura using the well-known counter as taught by Olarig to control the loading of a predetermined value by control logic for each thread in the memory, because by doing so, as suggested by Olarig the combined system would be able to use the counter to determine the overall priority level for a processing unit in a multiprocessing system and distribute the interrupt to that processing unit, therefore to balance the workload of the combined system [e.g., Olarig: col. 3, lines 18-38].

As to claim 11, this claim merely recited the same features as claim 20 with less limitations, hence are rejected for the same reason.

As to claims 13-19 and 21, in addition to the features of claims 11 and 20, Kimura and Olarig further disclosed that access to the resource is given to the thread with higher priority and the usage of the resource [e.g., Kimura: col. 4, line 64-col. 5, line 10; col. 6, lines 26-30], wherein the resource is a decode unit [Kimura: 1-3, Fig. 2; instruction decode units 1-3; Fig. 13; 111-113, Fig. 15] in a processor system, the

decode unit correspond to a bus unit [for example, Kimura: Internal Bus and Instruction Decode Units 1-3, Fig. 13] which including queues [for example, Kimura: 30, 40, 50, Fig. 2; 140, Fig. 15] to storing bus requests from a plurality of threads [Kimura: Fig. 2; Fig. 8; Fig. 11; Fig. 13] and control logic [Kimura: 60, Fig. 2; 60, 150, 170, Fig. 15] couple to the queues to select based on the priority value [Kimura: Fig. 2; Fig (s). 8-9; Fig. 11; Fig. 13; Fig. 15 and associated texts].

As to claims 1, 3-10, the steps in the claimed method is deemed to be made obvious by the functions of the apparatus structure of claims 11 and 13-20 in the combination discussed above, hence were rejected for the same reasons.

(10) Response to Argument

Applicant's arguments filed on Jan. 16, 2007 have been fully considered but they are not persuasive.

The examiner disagrees with appellant's piecemeal interpretation and arguments against the 35 U.S.C. § 103(a) rejections.

The Applicant's Invention:

A computer-implemented system and method that set up priorities for a plurality task threads.

Applicant argues that "Though counters are well know in the art, these is no description or suggestion in the Kimura and/or Olarig reference to provide a counter for

allocating resources in a multi-threaded environment as described in claim 1". The arguments are not persuasive.

In response to applicant's arguments, the examiner directs applicant's attention to the following disclosure excerpted form the prior art:

1) Kimura specifically discloses a single multithreaded processor for executing multiple instruction streams independently of each other. [e.g., Title, Abstract] wherein, the multithread processor comprises an instruction cache memory [e.g., the unit 100, Fig. 1] which coupled to a priority control unit [e.g., the unit 60, Fig. 1] to assign task executing priorities (or values) for each functional execution units of the multi-thread system via three registers including a priority designating registers [e.g., col. 8, lines 59 – col. 9, lines 8].

2) Olarig clearly discloses an I/O resource scalable (or selectable) multi-processor (MP) system which utilizes a counter of certain-bit length, wherein, the counter size is appended to a task priority register corresponding with a particular processing unit [e.g., col. 3, lines 30-33]. Olarig further clearly discloses that the contents of the task priority register and the counter size appended thereto are used to determine the overall priority level for that processing unit [e.g., col. 3, lines 33-35]. Moreover, Olarig clearly discloses an MP-compatible interrupt controller schema that apply the use of this bit-counter priority setting to selectively controls (or balances) the allocation (or distribution) of system resource per I/O interrupts [e.g., Olarig: Abstract, col. 3, lines 18 – 38; col. 4, lines 7-17, Fig(s). 3 & 5 and associated texts]. Hence, one of ordinary skill in the art at the time the invention was made would in fact, look to

incorporate the integrated MP-compatible interrupt controller schema to control the allocation of system resource to a bus agent [e.g., grant the bus 311 for message delivery at col. 9, lines 13-46] based on the "rotating priority" or "round robin" arbitration protocol that is integrated controlled by Local Programmable Interrupt Controllers [e.g., the LOPIC: 305, 306, Fig. 3] with their corresponding processing units including the bit-size counter [e.g., col. 6, lines 41-57] for masking a current –task-priority register [CTPR at col. 7, line 40, Fig.(s) 3 and 5 and associated texts]. Because by doing so, the combined system will be upgraded from a multi-thread single processor system to an complex Multi-Processors compatible system that would provide a cost-effective interrupt controller schema that guarantees a dynamic balanced allocation (or delivery) of system resource (or grant the bus 311 for message delivery at col. 9, lines 13-46] to a bus agent based on the task priority derived from the "rotating priority" or "round robin" arbitration logic control implemented by the bit-size counter. Therefore, contrary to applicant's arguments the examiner contends that the prior art on record in a combination clearly discloses the claimed counter used for allocating resources in a multi-threaded environment.

Based on the discussion above, because applicant does not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections.

allocating resources in a multi-threaded environment as described in claim 1". The arguments are not persuasive.

In response to applicant's arguments, the examiner directs applicant's attention to the following explanation and disclosure excerpted form the prior art:

1) Kimura specifically discloses a single multithreaded processor for executing multiple instruction streams independently of each other. [e.g., Title, Abstract] wherein, the multithread processor comprises an instruction cache memory [e.g., the unit 100, Fig. 1] which coupled to a priority control unit [e.g., the unit 60, Fig. 1] to assign task executing priorities (or values) for each functional execution units of the multi-thread system via three registers including a priority designating registers [e.g., col. 8, lines 59 – col. 9, lines 8].

2) Olarig clearly discloses an I/O resource scalable (or selectable) multi-processor (MP) system comprising at least three major I/O interrupt control handling threads [e.g., the units: 305, 306, 312, Fig. 3 and associated texts]. Each one of the three interrupt control processor utilizes a counter of certain-bit length, wherein, the counter size is appended to a task priority register corresponding with a particular processing unit [e.g., col. 3, lines 30-33]. Olarig further clearly discloses that the contents of the task priority register and the counter size appended thereto are used to determine the overall priority level for that processing unit [e.g., col. 3, lines 33-35]. Moreover, Olarig clearly discloses the MP-compatible interrupt controller schema in his system applies the use of this bit-counter priority setting to selectively control (or balance) the allocation (or distribution) of system resource [e.g., grant the bus 311 for

message delivery to an bust agent at col. 9, lines 13-46] per I/O interrupts requests submitted by a bus agent [e.g., Olarig: Abstract, col. 3, lines 18 – 38; col. 4, lines 7-17, Fig(s). 3 & 5 and associated texts]. Hence, one of ordinary skill in the art at the time the invention was made would in fact, look to incorporate the integrated MP-compatible interrupt controller schema to control (or balance) the allocation of system resource to a bus agent based on the "rotating priority" or "round robin" arbitration protocol that is integrated controlled by the Local/Central Programmable Interrupt Controllers [e.g., the LOPIC(s): 305, 306 & COPIC of Fig. 3] with their corresponding processing units including the wrapped-around value assigned to a bit-size counter [e.g., col. 6, lines 41-57] and the relative value assigned to a current–task-priority register [CTPR at col. 7, line 40, Fig.(s) 3 and 5 and associated texts] to determine the overall priority level of a processor, because by doing so, the combined system will be upgraded from a multi-thread single processor system to a more complex, advanced Multi-Processor, Multi-thread compatible system that guarantees a cost-effective solution providing an I/O interrupt controller schema for dynamically balancing the allocation (or delivery) of system resource [or dynamic selection among bus agents to grant a system resource " bus" for message delivery] based on the total task priority derived from the "rotating priority" or "round robin" arbitration logic control which is clearly archived by the use of a bit-size counter [Abstract, lines 8-13, col. 6, lines 41-57, col. 10, lines 21-36]. Therefore, contrary to applicant's arguments the examiner contends that the prior art on record in a combination clearly discloses the argued limitations.

Based on the discussion above, because applicant does not clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. Further, they do not show how the amendments avoid such references or objections. In addition, since applicant already got a patent (i.e., the patent No. 6,658,447) for the same invention and the instant application merely broader the claim scope and fails to advance the art, as such, even if a terminal disclaimer was filed on Oct. 28, 2005 to abolish the double patenting rejection on record, the examiner regards that the art rejection should be maintained.

For the above reasons, it is believed that the rejections should be sustained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

Respectfully submitted,

Susan Y Chen
Examiner
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Susan Chen

Conferees:

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